



P-Channel 1.8-V (G-S) MOSFET

CHARACTERISTICS

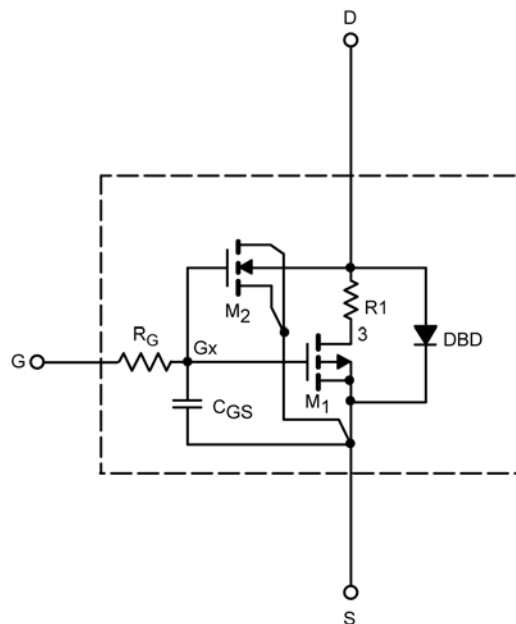
- P-Channel Vertical DMOS
- Macro Model (Subcircuit Model)
- Level 3 MOS
- Apply for both Linear and Switching Application
- Accurate over the -55 to 125°C Temperature Range
- Model the Gate Charge, Transient, and Diode Reverse Recovery Characteristics

DESCRIPTION

The attached spice model describes the typical electrical characteristics of the p-channel vertical DMOS. The subcircuit model is extracted and optimized over the -55 to 125°C temperature ranges under the pulsed 0-V to 5-V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage.

A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched C_{gd} model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

SUBCIRCUIT MODEL SCHEMATIC



This document is intended as a SPICE modeling guideline and does not constitute a commercial product data sheet. Designers should refer to the appropriate data sheet of the same number for guaranteed specification limits.

SPICE Device Model Si1405BDH



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SPECIFICATIONS ($T_J = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)					
Parameter	Symbol	Test Condition	Simulated Data	Measured Data	Unit
Static					
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = -250 \mu\text{A}$	0.83		V
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} \leq -5 \text{ V}, V_{GS} = -4.5 \text{ V}$	35		A
Drain-Source On-State Resistance ^a	$r_{DS(on)}$	$V_{GS} = -4.5 \text{ V}, I_D = -2.8 \text{ A}$	0.078	0.091	Ω
		$V_{GS} = -2.5 \text{ V}, I_D = -2.3 \text{ A}$	0.122	0.132	
		$V_{GS} = -1.8 \text{ V}, I_D = -0.50 \text{ A}$	0.178	0.171	
Forward Transconductance ^a	g_{fs}	$V_{DS} = -4 \text{ V}, I_D = -2.8 \text{ A}$	7.5	4.8	S
Diode Forward Voltage ^a	V_{SD}	$I_S = -1.4 \text{ A}$	-0.75	-0.80	V
Dynamic^b					
Input Capacitance	C_{iss}	$V_{DS} = -4 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$	332	305	pF
Output Capacitance	C_{oss}		108	108	
Reverse Transfer Capacitance	C_{rss}		61	66	
Total Gate Charge	Q_g	$V_{DS} = -4 \text{ V}, V_{GS} = -4.5 \text{ V}, I_D = -2.8 \text{ A}$	2.3	3.67	nC
Gate-Source Charge	Q_{gs}		0.61	0.61	
Gate-Drain Charge	Q_{gd}		0.98	0.98	

Notes

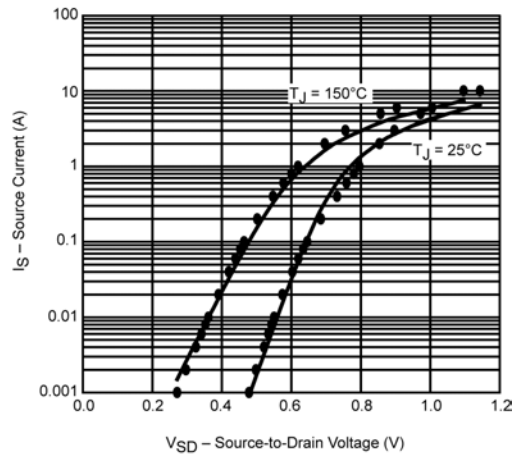
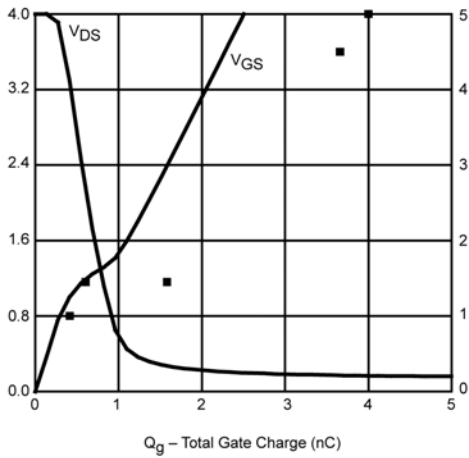
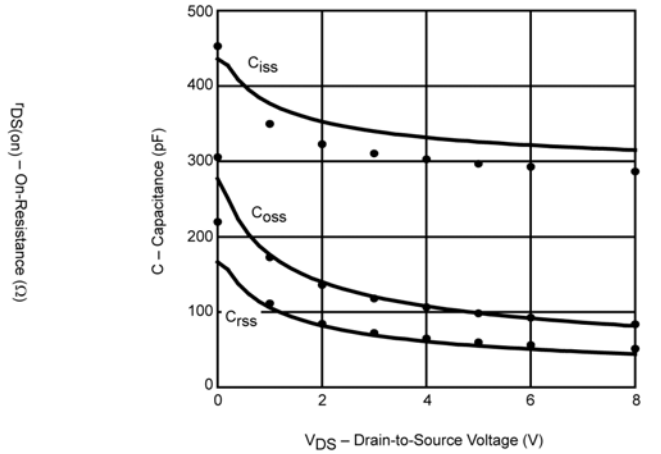
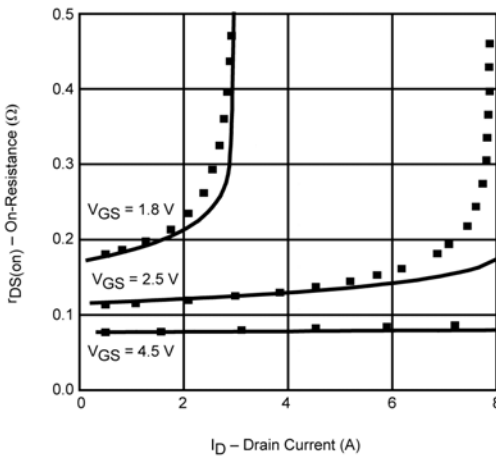
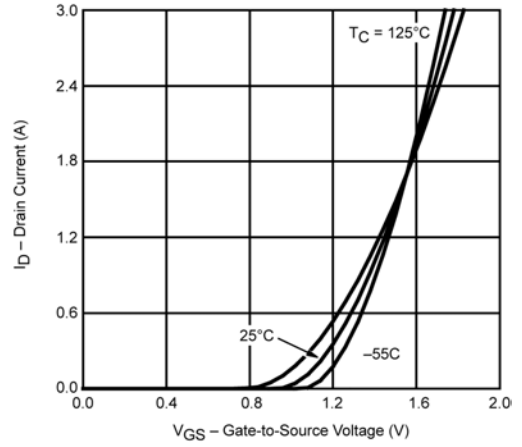
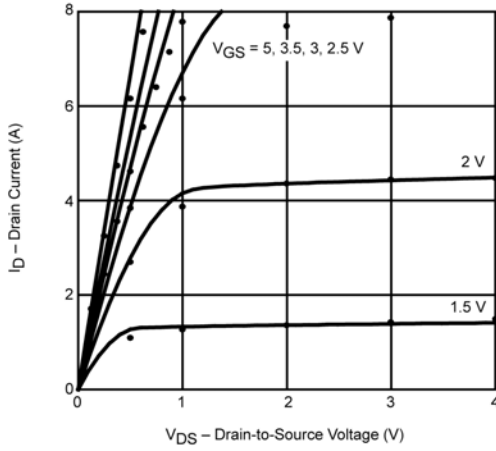
- a. Pulse test; pulse width $\leq 300 \mu\text{s}$, duty cycle $\leq 2\%$.
- b. Guaranteed by design, not subject to production testing.



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COMPARISON OF MODEL WITH MEASURED DATA ($T_J=25^\circ\text{C}$ UNLESS OTHERWISE NOTED)



Note: Dots and squares represent measured data.



Disclaimer

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